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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/034,070 | 12/20/2001 | Robert Kaiser | W&B-INF-952 | 9447 |

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| EXAMINER | |
|---|---|
| TRIMMINGS, JOHN P | |
| **ART UNIT** | **PAPER NUMBER** |
| 2133 | |

DATE MAILED: 03/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/034,070 | KAISER ET AL. | |
| | Examiner | Art Unit | |
| | John P Trimmings | 2133 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-10 and 12-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This Office Action is in response to the applicant's amendment dated 9/10/2004.

Claims 1, 4, 9, 10, 12 and 15 have been amended.

Claims 11 and 22 have been cancelled by the applicant.

Claims 1-10 and 12-21 are pending.

### *Response to Amendment*

1. In view of the applicant's amendment of Claims 4, 9, 10, 12 and 15, the examiner withdraws the rejections of said claims under 35 USC 112 second paragraph.

### *Response to Arguments*

2. In view of the amendments to Claims 1 and 12, applicant's arguments with respect to claims 1 and 12, and all independent claims thereof, have been considered but are moot in view of the new grounds of rejection. Applicant's amendment necessitated further consideration of reference art, because the scope of the two independent Claims 1 and 12 had been changed. The applicant is directed to the new rejections below.

### *Claim Rejections - 35 USC § 103*

3. Claims 1, 4-10, 12 and 15-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dreibelbis et al., "Processor-Based Built-In Self-Test for Embedded DRAM", in view of Wong, U.S. Patent No. 6363008.

As per Claims 1 and 12:

Dreibelbis et al. teaches an integrated circuit and methodology (see Abstract), comprising: a data processing unit (page 1732 column 1 paragraph 3, and column 2 paragraph 1); a buffer memory having registers for storing data for said data processing unit (FIG.2 Redundancy Allocation Register, and FIG.6(a) and (d) for example, Databit Redundancy Allocation Register), said buffer memory connected to said data processing unit (FIG.2 BIST Control Logic via Address/Data lines). The data in this buffer is serially passed on (see Abstract and page 1736 last paragraph), to be used by the circuit in determining which fuses are blown in repair of the memory (the address failure data is sent to the Fuser/Tester; page 1732 paragraph 3). Dreibelbis et al. further teaches a setting memory (FIG.6 Databit Fail Latch, and page 1736 column 2 paragraph 2) connected to the buffer memory (FIG.6 Databit Redundancy Allocation Register), the setting memory at least one of being written to (page 1735 column 2 paragraph 3) and being read from through said buffer memory. But Dreibelbis et al., even though it is taught that "fuses" are blown in the process, fails to teach that the setting memory "has an electrical fuse". But in the analogous art of Wong, this feature is suggested, where fuse blowing is accomplished in order to repair a bad memory with a redundant cell (column 5 line 30; "Such [poly fuses] fuses and similar structures are commonly employed for repair operations using redundant memory cells in conventional memory). The suggestion by Wong is that the repair data shifted in and out of Dreibelbis et al. is in fact data which is used in a fusing process for a setting memory (see Abstract). And, although the setting memory of Wong is not the same as

the setting memory of Dreibelbis et al., the process of fuse blowing for the purpose of correcting data failure is the teaching which Wong provides. And Wong, in column 2 lines 33-40, boasts of memories operable in multiple modes, thereby allowing for better utilization of manufactured product according to the quality. One with ordinary skill in the art at the t5ime of the invention, motivated as suggested, would have found it obvious to combine the technique of Wong to Dreibelbis et al. in order to increase production yield of memory circuits.

As per Claims 4 and 15:

The integrated circuit or method according to claim 1 or 12, is further limited wherein said processing unit has an arithmetic logic unit. Although the processor of Dreibelbis et al. does not specifically recite an ALU, ALUs are well known components of microprocessors. And one with ordinary skill in the art at the time of the invention, motivated by Dreibelbis et al. (Abstract) to provide powerful DRAM testing with minimum I/O pins by utilizing a processor, would have found it obvious to also have provided an ALU with the processor.

As per Claims 5 and 16:

Dreibelbis et al. further teaches the integrated circuit or method according to claim 4 or 15, wherein a register of said registers processes data (FIG.4 bits 0-31); and another register of said registers processes coded instructions for said arithmetic logic unit (FIG.4 bits 32-33). And in view of the motivation previously stated, the claims are rejected.

As per Claims 6 and 17:

Dreibelbis et al. further teaches the integrated circuit or method according to claim 5 or 16, wherein said buffer memory (FIG.6 (a) and (d)) is two buffer memories each containing data to be processed. And in view of the motivation previously stated, the claims are rejected.

As per Claims 7 and 18:

Dreibelbis et al. further teaches the integrated circuit or method according to claim 1 or 12, wherein said buffer memory is a latch (FIG.6 (d) Failed Word Address Counter). It is well known in the art that when a counter is not counting, it is a latch that holds the count. And in view of the motivation previously stated, the claims are rejected.

As per Claims 8 and 19:

Dreibelbis et al. further teaches the integrated circuit or method according to claim 1 or 12, wherein said buffer memory has a shift register (FIG.6 (a) scan in and scan out of Redundancy Allocation Registers). It is well known in the art that when a register scans in and out, it does so by means of a shift register. And in view of the motivation previously stated, the claims are rejected.

As per Claims 9 and 20:

Dreibelbis et al. further teaches the integrated circuit or method according to claim 8 or 19, wherein said shift register has at least one switch subdividing said shift register into registers for said processing unit. The two registers, Word Allocation and Bit Allocation are separate scanable registers and are switchable under control of Row or Databit Commit (FIG.6 (a)). And in view of the motivation previously stated, the claims are rejected.

As per Claims 10 and 21:

Dreibelbis et al. further teaches the integrated circuit or method according to claim 1 or 12, wherein said processing unit serially writes to and reads from each of said registers (FIG.2 between Sequencer and Redundancy Allocation, and see "Clock Generator" on page 1734). And in view of the motivation previously stated, the claims are rejected.

4. Claims 2-3 and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dreibelbis et al., "Processor-Based Built-In Self-Test for Embedded DRAM", in view of Wong, U.S. Patent No. 6363008 as applied to Claims 1 and 12 above, and further in view of Tsukakoshi et al., U.S. Patent No. 5337318.

As per Claims 2 and 13:

Dreibelbis et al. and Wong fail to further teach the integrated circuit and method according to claim 1 or 12, including circuit elements, said setting memory activating said circuit elements. However, in the analogous art of Tsukakashi et al., a setting memory (column 6 lines 39-40) activates redundant memory elements (column 4 lines 55-68 and column 5 lines 1-10). The advantage stated for this device is recited in column 1 lines 64-68 and column 2 lines 1-38 as being a way to quickly test for defective memory cells using several setting memories. One with ordinary skill in the art at the time of the invention would be motivated as suggested by Tsukakoshi et al. to combine the multiple setting memories of Tsukakoshi et al. with the system of Dreibelbis et al. in order to more quickly complete the testing of LSI memories.

As per Claims 3 and 14:

Tsukakoshi et al. further teaches the integrated circuit and method according to claim 2 or 13, including a memory having memory areas (column 1 lines 1-10), said circuit elements being memory elements used to replace at least one of said memory areas (see Abstract). And in view of the motivation previously stated in Claim 2 or 13, the claims are rejected.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is (571)

272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

jpt

Gregory J. Lamarre
Primary Examiner